Express Mail" Label No. EL 889366545 US
Date of Deposit: March 14, 2002

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Address" service under 37 CFR 1.10 on the date indicated above and is addressed to:

Assistant Commission for Patents
Washington, DC 20231

TOWNSEND and TOWNSEND and CREW LLP

By: Maisie C. Livengood
Maisie C. Livengood

PATENT
Attorney Docket No.: 00939s-050510US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Michael J. Peters, et al.

Application No.: TO BE ASSIGNED

Filed: HEREWITH

For: INTEGRATED CIRCUIT I/O PAD CELL MODELING

Art Unit:

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced application, please enter the following amendments and remarks.

IN THE SPECIFICATION:

Please amend the specification as follows. A marked-up version of the amended paragraphs is attached hereto as Appendix A.

Please insert the following sentence at the top of the specification:

--This application is a division of U.S. application no. 08/299,395, filed September 1, 1994.--

Please replace the paragraph beginning at page 4, line 20 with the following rewritten paragraph:

--Figures 10A-10C show a design methodology for designing and fabricating integrated circuit devices.--

Please replace the paragraph beginning at page 4, line 37 with the following rewritten paragraph:

--Figures 10A-10C show a typical design methodology for designing integrated circuits, and in particular for designing ASICs. First, initial planning of the design is done at 90. The design is then entered at 91 using standard CAE/CAD tools known in the industry, such as those from Cadence Design Systems, Mentor Graphics, Synopsis and Viewlogic. Part of logic entry includes compiling the pad cells, using an I/O compiler such as the VS500 I/O Compiler, available from AT&T Global Information Solutions Company, Microelectronics Division located in Ft. Collins, Colorado (hereinafter AT&T MPD). After design entry, the user can optionally perform static timing analysis at 92 (using a tool such as VeriTime, available from Cadence Design Systems, Inc. which is located in San Jose, California), as well as generate input stimulus waveforms at 93 for use in subsequence simulation (using a tool such as Wisil, also available from AT&T MPD). After such stimulus waveform creation, the user can optionally perform functional simulations at 94. The user then performs real time simulation at 95 using the same simulator. These simulation steps are where the present invention is utilized. The particular model detailed herein was written for use with the Verilog simulator, such simulator being available from Cadence Design Systems. After simulation, power analysis can optionally be performed at 96 using a PowerCalc tool, available from AT&T MPD. The simulation results are then validated at 97, preferably with the Verify design test tool (also available from AT&T MPD). A net checking tool called NetChecker (also available from AT&T MPD) can then be run at 98. The layout 99, post-layout verification 100 and prototype 101 phases shown in Figure 10C are standard in the industry, and are not important to the understanding of the present invention described herein.--

IN THE CLAIMS:

Please substitute the following claims 1, 2, 3, 8, and 9 for the pending claims of the same number. Please cancel claims 4-7, 11 and 12. Please add new claims 13-17. A marked-up version of the amended claims is attached hereto as Appendix A and a clean version of all pending claims is attached hereto as Appendix B.

1. (Amended) A system for modeling a bi-directional signal of an electric circuit, comprising:

means for maintaining a first value representing an input component of the bi-directional signal;

means for maintaining a second value representing an output component of the bi-directional signal; and

means for generating a third value based upon at least the first value and second value.

2. (Amended) The system of Claim 1 wherein the means for generating a third value is further based upon resistive data.

3. (Amended) The system of Claim 1 wherein the first value, second value and third value are output to a computer file.

8. (Amended) A method for modeling a bi-directional signal of an electric circuit, comprising:

maintaining a first value representing an input component of the bi-directional signal;

maintaining a second value representing an output component of the bi-directional signal; and

generating a third value based upon at least the first value and second value.

9. (Amended) The method of Claim 8 wherein the third value is further based upon resistive data which models at least a portion of resistance coupled to a pad cell.

10. (Amended) The method of Claim 8 further comprising:

specifying at least one bi-directional signal of a logic design to be simulated; and

simulating the logic design.

13. (New) A method for generating a simulation output file, comprising:

placing first data in the simulation file which represents when an input signal applied to a bi-directional pad is de-asserted; and

placing second data in the simulation file which represents when an output signal applied to the bi-directional pad is asserted.

14. (New) The method of Claim 13 further comprising:

placing third data in the simulation file which represents when a resolved signal is asserted, the resolved signal being a combination of the input signal applied to the bi-directional pad, the output signal applied to the bi-directional pad, and a resistance value associated with the bi-directional pad.

15. (New) A simulation model for a bi-directional pad, said simulation model being responsive to an applied stimulus and generating responses thereto, and having at least two modes of operation, where a first mode of operation provides at least two response values for the bi-directional pad, and a second mode of operation provides at least three response values for the bi-directional pad.

16. (New) A method for operating an improved pad cell model, comprising:

maintaining a first value representing an input component of the bi-directional signal;

maintaining a second value representing an output component of the bi-directional signal; and

generating a third value based upon at least the first value and second value.

17. (New) The method of claim 16, wherein the improved pad cell model comprises:

an input node having a value which reflects data that is supplied to the pad cell from external sources;

an output node having a value which reflects data that is supplied as output from the pad cell; and

a resolved node, coupled to the input node and output node, having a value which reflects a combination of the input node value and the output node value.

REMARKS

The application claims priority from U.S. application no. 08/299,395. The 08/299,395 case was appealed to the Board of Patent Appeals and Interferences. A Decision on Appeal in that case was issued on November 7, 2001. It is worth noting that, in regard to the cited Agrawal reference (Agrawal et al., "Can Logic Simulators Handle Bidirectionality and Charge Sharing?", 1990 IEEE Int'l Symposium on Circuits and Systems, vol. 1, at 411-14 (May 1990)), the Board found that the Agrawal reference did not disclose the combination of the values of the input node and the output node.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

Chad E. King
Reg. No. 44,187

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
CEK/mcl
DE 7062618 v1

Appendix A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The following paragraph has been inserted at the beginning of the Specification:

This application is a division of U.S. application no. 08/299,395, filed September 1, 1994.

Paragraph beginning at line 20 of page 4 has been amended as follows:

~~Figure 10 shows~~ Figures 10A-10C show a design methodology for designing and fabricating integrated circuit devices.

Paragraph beginning at line 37 of page 4 has been amended as follows:

~~Figure 10 shows~~ Figures 10A-10C show a typical design methodology for designing integrated circuits, and in particular for designing ASICs. First, initial planning of the design is done at 90. The design is then entered at 91 using standard CAE/CAD tools known in the industry, such as those from Cadence Design Systems, Mentor Graphics, Synopsis and Viewlogic. Part of logic entry includes compiling the pad cells, using an I/O compiler such as the VS500 I/O Compiler, available from AT&T Global Information Solutions Company, Microelectronics Division located in Ft. Collins, Colorado (hereinafter AT&T MPD). After design entry, the user can optionally perform static timing analysis at 92 (using a tool such as VeriTime, available from Cadence Design Systems, Inc. which is located in San Jose, California), as well as generate input stimulus waveforms at 93 for use in subsequence simulation (using a tool such as Wisil, also available from AT&T MPD). After such stimulus waveform creation, the user can optionally perform functional simulations at 94. The user then performs real time simulation at 95 using the same simulator. These simulation steps are where the present invention is utilized. The particular model detailed herein was written for use with the Verilog simulator, such simulator being available from Cadence Design Systems. After

simulation, power analysis can optionally be performed at 96 using a PowerCalc tool, available from AT&T MPD. The simulation results are then validated at 97, preferably with the Verify design test tool (also available from AT&T MPD). A net checking tool called NetChecker (also available from AT&T MPD) can then be run at 98. The layout 99, post-layout verification 100 and prototype 101 phases shown in Figure 10C are standard in the industry, and are not important to the understanding of the present invention described herein.

IN THE CLAIMS:

The claims have been amended as follows:

1. (Amended) A system for modeling a bi-directional signal of an electric circuit, comprising:

means for maintaining a ~~state of~~ first value representing an input component of the bi-directional signal;

means for maintaining a ~~state of~~ second value representing an output component of the bi-directional signal; and

means for generating a ~~resolved state~~ third value based upon at least the ~~input component state and output component state~~ first value and second value.

2. (Amended) The system of Claim 1 wherein the ~~resolved state~~ means for generating a third value is further based upon resistive data.

3. (Amended) The system of Claim 1 wherein the ~~input component state, output component state and resolved state~~ first value, second value and third value are output to a computer file.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Amended) A method for modeling a bi-directional signal of an electric circuit, comprising ~~the steps of~~:

maintaining a ~~state of~~ first value representing an input component of the bi-directional signal;

maintaining a ~~state of~~ second value representing an output component of the bi-directional signal; and

generating a ~~resolved value~~ third value based upon at least the ~~input component state and output component state~~ first value and second value.

9. (Amended) The method of Claim 8 wherein the ~~resolved state~~ third value is further based upon resistive data which models at least a portion of resistance coupled to a pad cell.

10. (Amended) The method of Claim 8 further comprising ~~the steps of~~:

specifying at least one bi-directional signal of a logic design to be simulated; and

simulating the logic design.

11. (Canceled)

12. (Canceled)

13. (New) A method for generating a simulation output file, comprising:

placing first data in the simulation file which represents when an input signal applied to a bi-directional pad is de-asserted; and

placing second data in the simulation file which represents when an output signal applied to the bi-directional pad is asserted.

14. (New) The method of Claim 13 further comprising:

placing third data in the simulation file which represents when a resolved signal is asserted, the resolved signal being a combination of the input signal applied to the bi-directional pad, the output signal applied to the bi-directional pad, and a resistance value associated with the bi-directional pad.

15. (New) A simulation model for a bi-directional pad, said simulation model being responsive to an applied stimulus and generating responses thereto, and having at least two modes of operation, where a first mode of operation provides at least two response values for the bi-directional pad, and a second mode of operation provides at least three response values for the bi-directional pad.

16. (New) A method for operating an improved pad cell model, comprising:

maintaining a first value representing an input component of the bi-directional signal;

maintaining a second value representing an output component of the bi-directional signal; and

generating a third value based upon at least the first value and second value.

17. (New) The method of claim 16, wherein the improved pad cell model comprises:

an input node having a value which reflects data that is supplied to the pad cell from external sources;

an output node having a value which reflects data that is supplied as output from the pad cell; and

a resolved node, coupled to the input node and output node, having a value which reflects a combination of the input node value and the output node value.

Appendix B

PENDING CLAIMS

1. (Amended) A system for modeling a bi-directional signal of an electric circuit, comprising:

means for maintaining a first value representing an input component of the bi-directional signal;

means for maintaining a second value representing an output component of the bi-directional signal; and

means for generating a third value based upon at least the first value and second value.

2. (Amended) The system of Claim 1 wherein the means for generating a third value is further based upon resistive data.

3. (Amended) The system of Claim 1 wherein the first value, second value and third value are output to a computer file.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Amended) A method for modeling a bi-directional signal of an electric circuit, comprising:

maintaining a first value representing an input component of the bi-directional signal;

maintaining a second value representing an output component of the bi-directional signal; and

generating a third value based upon at least the first value and second value.

9. (Amended) The method of Claim 8 wherein the third value is further based upon resistive data which models at least a portion of resistance coupled to a pad cell.

10. (Amended) The method of Claim 8 further comprising:

specifying at least one bi-directional signal of a logic design to be simulated; and

simulating the logic design.

11. (Canceled)

12. (Canceled)

13. (New) A method for generating a simulation output file, comprising:

placing first data in the simulation file which represents when an input signal applied to a bi-directional pad is de-asserted; and

placing second data in the simulation file which represents when an output signal applied to the bi-directional pad is asserted.

14. (New) The method of Claim 13 further comprising:

placing third data in the simulation file which represents when a resolved signal is asserted, the resolved signal being a combination of the input signal applied to the bi-directional pad, the output signal applied to the bi-directional pad, and a resistance value associated with the bi-directional pad.

15. (New) A simulation model for a bi-directional pad, said simulation model being responsive to an applied stimulus and generating responses thereto, and having at least two modes of operation, where a first mode of operation provides at least two response values for the

bi-directional pad, and a second mode of operation provides at least three response values for the bi-directional pad.

16. (New) A method for operating an improved pad cell model, comprising:

maintaining a first value representing an input component of the bi-directional signal;

maintaining a second value representing an output component of the bi-directional signal; and

generating a third value based upon at least the first value and second value.

17. (New) The method of claim 16, wherein the improved pad cell model comprises:

an input node having a value which reflects data that is supplied to the pad cell from external sources;

an output node having a value which reflects data that is supplied as output from the pad cell; and

a resolved node, coupled to the input node and output node, having a value which reflects a combination of the input node value and the output node value.